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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,454	08/24/2001	Kai-Yeung (Sunny) Siu	SLKN-001/01US	3653

23419 7590 08/22/2005

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EXAMINER	
NGUYEN, PHUONGCHAU BA	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,454	SIU ET AL.	
	Examiner	Art Unit	
	Phuongchau Ba Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2-13-2,6-11-2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Objections

1. Claims 3, 6, 28 are objected to because of the following informalities: ":" should be deleted. Appropriate correction is required.

Double Patenting

2. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

3. Claims 26-39 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 26-29 of copending Application No. 09/939,464. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

4. Claims 1-50 are provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-50 of copending Application No. 09/940,148. This is a provisional double patenting rejection since the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4, 7,19, 20, 22-25, 30-38, 42, 50 are rejected under 35 U.S.C. 102(b) as being anticipated by Brown (5,896,380).

Regarding claim 1,

Brown (5,896,380) discloses a network switch (figs.1, 3), comprising:

an input layer (I/P fabric 12-fig.1) including N input layer circuits, each input layer circuit including an input layer circuit input port (fig.1) and N queues (queues 54-fig.3) corresponding to N output terminals (fig.1);

an intermediate layer (core fabric 18-fig.1) including N intermediate layer circuits, each intermediate layer circuit including N buffers (queues 64-fig.3) positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals (fig.1); and

an output layer (O/P fabric 22-fig.1) including N output layer circuits, each output layer circuit having N output layer circuit input terminals and an output layer circuit output port, said N output layer circuit input terminals corresponding to individual intermediate layer circuit output terminals of said N intermediate layer circuits (fig.1).

Regarding claims 2 & 23,

Brown further discloses wherein each input layer circuit includes

a sorting circuit (inlet stage queuer 56-fig.3) to route incoming cells to one of N destinations, each destination of said N destinations having a corresponding queue within said input layer circuit (col.4, lines 44-49), and

a transposer circuit (scheduler 58-fig.3) coupled to said N queues and said N output terminals, said transposer circuit being configured to transpose cells stored in said N queues for delivery to said N output terminals (col.4, lines 50-55).

Regarding claims 3 & 24,

Brown further discloses wherein each intermediate layer circuit includes

a sorting circuit (controller 68-fig.3) to route incoming cells to said N buffers, said N buffers thereafter delivering said incoming cells to said N intermediate layer circuit output terminals (col.4, lines 62-65).

Regarding claims 4 & 25,

Brown further discloses wherein each output layer circuit includes:

a transposer circuit (controller 78-fig.3) coupled to said N output layer circuit input terminals, said transposer circuit being configured to transpose data cells received at said N output layer circuit input terminals (col.5, lines 5-8); and

an output layer circuit queue (queues 74-fig.3) coupled to said transposer circuit and said output layer circuit output port.

Regarding claim 7,

Brown (5,896,380) discloses a network switch, comprising:

an input layer (I/P fabric12-fig.1) to receive a data stream including a set of cells, each cell including data and a header to desire at a destination device, said input layer including a set of input layer circuits, a selected input layer circuit (queuer 56-fig.3) of said set of input layer circuits receiving said data stream, said selected input layer circuit including a set of queues (queues 54-fig.3) corresponding to a set of destination devices, said selected input layer circuit being configured to assign a selected cell from said data stream to a selected queue of said set of queues, said selected queue corresponding to a selected destination device specified by said header of said selected cell (col.4, lines 41-55);

an intermediate layer (core fabric 18-fig.1) including a set of intermediate layer circuits, each intermediate layer circuit including a set of buffers (queues 64-fig.3) corresponding to said set of destination devices, a selected intermediate layer circuit (queuer 66-fig.3) of said set of intermediate layer circuits receiving said selected cell and assigning said selected cell to a selected buffer corresponding to said selected destination device; and

an output layer (O/P fabric 22-fig.1) including a set of output layer circuits corresponding to said set of destination devices, a selected output layer circuit (queuer 76-fig.3) of said set of output layer circuits storing said selected cell prior to routing said selected cell to a selected output layer circuit output node.

Regarding claim 19,

Brown further discloses wherein said intermediate layer processes cells without communicating between said intermediate layer circuits (abstract, lines 14-18).

Regarding claim 20,

Brown further discloses wherein said set of intermediate layer circuits process cells in accordance with a link skew value and synchronization skew value (col.4, lines 63-65).

Regarding claim 22,

Brown (5,896,380) discloses a network switch, comprising:

an input layer (I/P fabric 12-fig.1) including N input circuits each coupled to an input port and having N buffers (queues 54-fig.3) therein corresponding to N output terminals;

an intermediate layer (core fabric 18-fig.1) including N intermediate circuits each having N input terminals and N output terminals, where the first output terminal of each input circuit is coupled to the first intermediate circuit and the Nth output terminal of each input circuit is coupled to the Kth intermediate circuit, where K=(1, 2, . . . N) (see also fig.3); and

an output layer (O/P fabric 22-fig.1) including N output circuits each having N input terminals and an output port, where the first output terminal of each intermediate circuit is coupled to the first output circuit and the Nth output terminal of each

intermediate circuit is coupled to the Lth output circuit, where L = (1, 2, . . . N) (see also fig.3).

Regarding claim 30,

Brown (5,896,380) discloses a network switch, comprising:

an input layer (I/P fabric 12-fig.1) including N input layer circuits, each input layer circuit including an input layer circuit input port and N queues (queues 54-fig.3) corresponding to N output terminals,

a sorting circuit (queuer 66-fig.3) to route incoming cells to one of N destinations, each destination of said N destinations having a corresponding queue within said input layer circuit, and

a transposer circuit (core controller 68-fig.3) coupled to said N queues and said N output terminals, said transposer circuit being configured to transpose cells stored in said N queues for delivery to said N output terminals.

Regarding claim 31,

Brown further discloses wherein said transposer circuit transposes said cells stored in said N queues for parallel delivery to said N output terminals (abstract, lines 7-18).

Regarding claim 32,

Brown further discloses an intermediate layer including N intermediate layer circuits (20-1 to 20-n, fig.3), each intermediate layer circuit including N buffers positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals (fig.3).

Regarding claim 33,

Brown further discloses an output layer (output stage) including N output layer circuits, each output layer circuit (each output stage fabric) having N output layer circuit input terminals (col.4, lines 64-65) and an output layer circuit output port (30-fig.3), said N output layer circuit input terminals corresponding to individual intermediate layer circuit output terminals of said N intermediate layer circuits (col.4, lines 64-65).

Regarding claim 34,

Brown (5,896,380) discloses a network switch, comprising:

an intermediate layer (core fabric 18-fig.1 & 3) including N intermediate layer circuits, each intermediate layer circuit including N buffers (queues 64-fig.3) positioned between N intermediate layer circuit input terminals and N intermediate layer circuit output terminals, said N intermediate layer circuits asynchronously receiving cells at said intermediate layer circuit input terminals and asynchronously delivering cells to said intermediate layer circuit output terminals.

Regarding claim 35,

Brown further discloses wherein each intermediate layer circuit (core stage fabric) includes a sorting circuit (core stage queuer 66-fig.3) to route incoming cells to said N buffers, said N buffers thereafter delivering said incoming cells to said N intermediate layer circuit output terminals.

Regarding claim 36,

Brown (5,896,380) discloses a network switch, comprising:

an output layer (O/P fabric 22-fig.1 & 3) including N output layer circuits, each output layer circuit having N output layer circuit input terminals and an output layer circuit output port each output layer circuit asynchronously receiving cells at said N output layer circuit input terminals and producing a serial cell stream at said output layer circuit output port.

Regarding claim 37,

Brown further discloses wherein each output layer circuit includes:

a transposer circuit (controller 78-fig.3) coupled to said N output layer circuit input terminals, said transposer circuit being configured to transpose data cells received at said N output layer circuit input terminals; and

an output layer circuit queue (queues 74-fig.3) coupled to said transposer circuit and said output layer circuit output port, said output layer circuit queue producing said serial cell stream.

Regarding claim 38,

Brown (5,896,380) discloses a method of routing network traffic, comprising:

receiving a data stream of cells at an input layer, each cell of said data stream of cells including data and a header to designate a destination device (abstract, lines 3-5);

routing a selected cell from said input layer to a selected intermediate layer circuit within a set of intermediate layer circuits, said routing including routing said selected cell to a specified buffer within said selected intermediate layer circuit that corresponds to said destination device of said selected cell (abstract, lines 3-21); and

delivering said selected cell from said selected intermediate layer circuit to a selected output layer circuit within a set of output layer circuits, said selected output layer circuit corresponding to said destination device of said selected cell (abstract, lines 3-21).

Regarding claim 42,

Brown (5,896,380) discloses a method of routing network traffic, said method comprising:

receiving a data stream with a set of cells, each cell including data and a header to designate a destination device (col.2, lines 43-46),

assigning a selected cell of said set of cells to a selected queue of a set of queues within an input layer circuit, said selected cell specifying a selected destination device, said selected queue corresponding to said selected destination device (col.2, lines 43-46);

routing said selected cell to a selected intermediate layer circuit within a set of intermediate layer circuits, said selected intermediate layer circuit including a set of buffers (queues 64-fig.3) corresponding to a set of destination devices, said selected intermediate layer circuit assigning said selected cell to a selected buffer of said set of buffers, said selected buffer corresponding to said selected destination device (col.2, lines); and

sending said selected cell to a selected output layer circuit within a set of output layer circuits, said selected output layer circuit corresponding said selected destination device, said selected output layer circuit storing said selected cell prior to delivering said selected cell to an output node (col.2, lines 50-55).

Regarding claim 50,

Brown further discloses wherein said sending includes sending said selected data cell from said selected intermediate layer circuit without communicating timing information with other intermediate layer circuits within said set of intermediate layer circuits (col.4, lines 63-65).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 6, 16, 39, 40, 44, 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (5,896,380) in view of Lipp (6,751,219).

Regarding claims 6, 16, 39, 44,

Brown discloses all the claimed limitations, except wherein said intermediate layer is configured to identify a multicast demand signal in a cell and thereafter replicate said cell to produce a multicast signal.

However, in the same field of endeavor, Lipp (6,751,219) discloses wherein said intermediate layer is configured to identify a multicast demand signal in a cell and thereafter replicate said cell to produce a multicast signal (col.20, lines 26-58).

Therefore, it would have been obvious to an artisan to apply Lipp's teaching to Brown's system with the motivation being to avoid localized congestion and packet blocking.

9. Claims 8-10, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (5,896,380) in view of Yang (6,570,854).

Regarding claim 8,

Brown discloses all the claimed limitations, except wherein said selected output layer circuit includes circuitry (35-36, fig.3) to generate a flow control warning signal for application to said selected input layer circuit.

However, in the same field of endeavor, Yang (6,570,854) discloses wherein said selected output layer circuit includes circuitry to generate a flow control warning signal for application to said selected input layer circuit (col.4, line 38-col.5, line 12).

Therefore, it would have been obvious to an artisan to apply Yang's teaching to Brown's system with the motivation being to prevent the switch being overloaded.

Regarding claim 9,

Brown discloses all the claimed limitations, except a line card connected to said selected input layer circuit, wherein said selected output layer circuit includes circuitry to generate a flow control warning signal for application to said line card.

However, in the same field of endeavor, Yang (6,570,854) discloses a line card (35-36, fig.3) connected to said selected input layer circuit, wherein said selected output layer circuit includes circuitry to generate a flow control warning signal for application to said line card (col.4, line 38-col.5, line 12).

Therefore, it would have been obvious to an artisan to apply Yang's teaching to Brown's system with the motivation being to prevent the switch being overloaded.

Regarding claim 10,

Brown discloses all the claimed limitations, except wherein said line card delivers only high priority cells to said input layer circuit in response to said flow control warning signal.

However, in the same field of endeavor, Yang (6,570,854) discloses said line card delivers only high priority cells to said input layer circuit in response to said flow control warning signal (col.1, line 39-col.2, line 12).

Therefore, it would have been obvious to an artisan to apply Yang's teaching to Brown's system with the motivation being to prevent the switch being overloaded.

Regarding claim 47,

Brown discloses all the claimed limitations, except generating a flow control signal at said selected output layer circuit; forming a flow control header signal within a header of an incoming data cell in response to said flow control signal; and processing said incoming data cell through said selected intermediate layer circuit and said selected output layer circuit in accordance with said flow control header signal.

However, in the same field of endeavor, Yang (6,570,854) discloses generating a flow control signal at said selected output layer circuit (FRM from source); forming a flow control header signal within a header of an incoming data cell in response to said flow control signal (BRM from destination); and processing said incoming data cell through said selected intermediate layer circuit and said selected output layer circuit in accordance with said flow control header signal (col.1, line 59-col.2, line 12). Therefore, it would have been obvious to an artisan to apply Yang's teaching to Brown's system with the motivation being to prevent the switch being overloaded.

10. Claims 12 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (5,896,380) in view of Nicols (6,473,428).

Regarding claim 12,

Brown discloses all the claimed limitations, except wherein said input layer includes circuitry to identify cell priority values within cell headers.

However, in the same field of endeavor, Nicols (6,473,428) discloses circuitry (queue engine 1002-fig.10) to identify (queue) cell priority values (high or low priority) within cell headers (col.7, lines 5-62). Therefore, it would have been obvious to an artisan to apply Nicols's teaching to Brown's system to maintain correct temporal ordering at the output port.

Regarding claim 43,

Brown discloses all the claimed limitations, except wherein said routing is initiated when said selected queue reaches a specified cell volume level.

However, in the same field of endeavor, Nicols (6,473,428) discloses wherein said routing is initiated when said selected queue reaches a specified cell volume level (col.5, lines 24-38). Therefore, it would have been obvious to an artisan to apply Nichols's teaching to Brown's system with the motivation being to prevent overloading at buffer.

11. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (5,896,380) in view of Nicols (6,473,428) as applied to claim 12 above, and further in view of Pelissier (6,661,773).

Regarding claim 13,

Brown discloses all the claimed limitations, except wherein said input layer alters delivery of cells in response to said cell priority values.

However, in the same field of endeavor, Pelissier (6,661,773) discloses wherein said input layer alters delivery of cells in response to said cell priority values (col.4, lines 4-23). Therefore, it would have been obvious to an artisan to apply Pelissier's teaching to Brown's system with the motivation being to provide a more flexible, cost effective, and performance-efficient technique for recovery from fault within a network infrastructure.

12. Claims 14-15, 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (5,896,380) in view of Plelissier (6,661,773).

Regarding claims 14, 48-49,

Brown discloses all the claimed limitations, except wherein said input layer is operative in a normal mode to deliver data cells to each of said intermediate layer circuits and is alternately operative in a fault mode to deliver cells to a subset of said intermediate layer circuits that remain operative.

However, in the same field of endeavor, Plelissier (6,661,773) discloses wherein said input layer is operative in a normal mode to deliver data cells to each of said

intermediate layer circuits and is alternately operative in a fault mode to deliver cells to a subset of said intermediate layer circuits that remain operative (col.4, lines 4-54). Therefore, it would have been obvious to an artisan to apply Plelissier's teaching to Brown's system with the motivation being to ensure data successfully delivered to respective destination nodes in the network.

Regarding claim 15,

Brown discloses all the claimed limitations, except wherein said intermediate layer is operative in a normal mode to deliver data cells to each of said output layer circuits and is alternately operative in a fault mode to deliver cells to a subset of said set of output layer circuits that remain operative.

However, in the same field of endeavor, Plelissier (6,661,773) discloses wherein said intermediate layer is operative in a normal mode to deliver data cells to each of said output layer circuits and is alternately operative in a fault mode to deliver cells to a subset of said set of output layer circuits that remain operative (col.4, lines 4-54). Therefore, it would have been obvious to an artisan to apply Plelissier's teaching to Brown's system with the motivation being to ensure data successfully delivered to respective destination nodes in the network.

13. Claims 17-18, 41, 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (5,896,380) in view of Milway (6,122,279).

Regarding claim 17,

Brown discloses all the claimed limitations, except wherein said intermediate layer circuit includes a first set of buffers to process high priority traffic and a second set of buffers to process best effort traffic.

However, in the same field of endeavor, Milway (6,122,279) discloses wherein said intermediate layer circuit (switch) includes a first set of buffers (480-HI FIFO-fig.4) to process high priority traffic and a second set of buffers (485-LO FIFO-fig.4) to process best effort traffic (col.17, lines 8-44). Therefore, it would have been obvious to an artisan to apply Milway's teaching to Brown's system with the motivation being to avoid significant delay or delay jitter to high priority data such as video and audio stream.

Regarding claim 18,

Brown discloses all the claimed limitations, except wherein said output layer includes a first set of output layer circuits to process said high priority traffic and a second set of output layer circuits to process said best effort traffic.

However, in the same field of endeavor, Milway (6,122,279) discloses wherein said output layer includes a first set of output layer circuits (480-Hi-fig.4) to process said high priority traffic and a second set of output layer circuits (485-Lo-fig.4) to process said best effort traffic (col.17, lines 8-44). Therefore, it would have been obvious to an

artisan to apply Milway's teaching to Brown's system with the motivation being to avoid significant delay or delay jitter to high priority data such as video and audio stream.

Regarding claims 41 & 46,

Brown discloses all the claimed limitations, except wherein said routing includes routing said selected cell to a dedicated high priority traffic intermediate layer circuit when said header specifies that said selected cell has a high priority.

However, in the same field of endeavor, Milway discloses wherein said routing includes routing said selected cell to a dedicated high priority traffic intermediate layer circuit when said header specifies that said selected cell has a high priority (col.17, lines 34-37). Therefore, it would have been obvious to an artisan to apply Milway's teaching to Brown's system with the motivation being to provide a service to urgent traffic in a more timely manner.

Allowable Subject Matter

14. Claims 5, 11, 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Claims 26-29 would be allowable if overcome double patenting rejection as set forth above.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuongchau Ba Nguyen whose telephone number is 571-272-3148. The examiner can normally be reached on Monday-Friday from 10:00 a.m. to 2:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PN

Phuongchau Ba Nguyen
Examiner
Art Unit 2665

DUC HO
PRIMARY EXAMINER

8-18-05